Transfer Characteristic and Device Quality of PTA10 Gated Field Effect Transistor (FET) for One Transistor (1T) of FRAM Applications

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Abstract

The aim of this work was the understanding of the mechanism that gave place to the improvement of the transfer characteristics of lead-based titanate TFT(PTA), in order to allow their application in 1T of FRAM. The transfer characteristic graphs were parabolic variation nature. The mth power of I_{DS} was evaluated and the values were not much difference for all TFT cells. $I_D^{\frac{1}{m}}$ and V_{GS} characteristics were also analyzed for identifying the transconductance values. According to the results obtained, the fabricated cells were said to be n – channel E-mode 1T of FeFET.

Keywords: TFT, PTA, Lead- based titanate, `FRAM

INTRODUCTION

In recent years, ferroelectric films have been studied for ferroelectric random access memories (FeRAM) application. Particularly, FET-type memory has received great attention of a next generation memory. FET-type ferroelectric memory has been expected to enable capability of multi-application IC card and portable terminal unit.

Experimental Procedure

To get the precursor solution, the raw materials of PbO, TiO_2, and Al_2O_3 were chosen as starting materials. Firstly, these powder materials were weighed and mixed to get the chemical formula $PbTi_{1-x} Al_x O_3$ (x = 0.10 mol %). Then, a few amount of acetone was added into the mixture and stirred with glass stirrer to be homogeneous. Primary ball-milling was carried out for 30 minutes. The homogeneous powder was sintered at 700ºC for 1hr in O_2 atmosphere. The secondary ball-milling was performed to get crystalline powder. It was mixed with 2-methoxyethanol solvent to change into liquid phase and refluxed up to 100ºC for 30 min. After drying, it became precursor solution and ready to deposit onto desired substrate. The p-type Si (100) orientations were chosen as starting substrates to get n-channel TFTs. They were cleaned with a dilute solution of HF: DIW (1:5), acetone and methyl alcohol to remove native contamination and dried at room temperature. SiO_2's were thermally deposited on all p-Si(100) wafers. The middle zones of the insulating layers grown on Si wafers were covered with apiezon wax and their ends were etched with HF: DIW (1:3) to remove SiO_2 layers totally.

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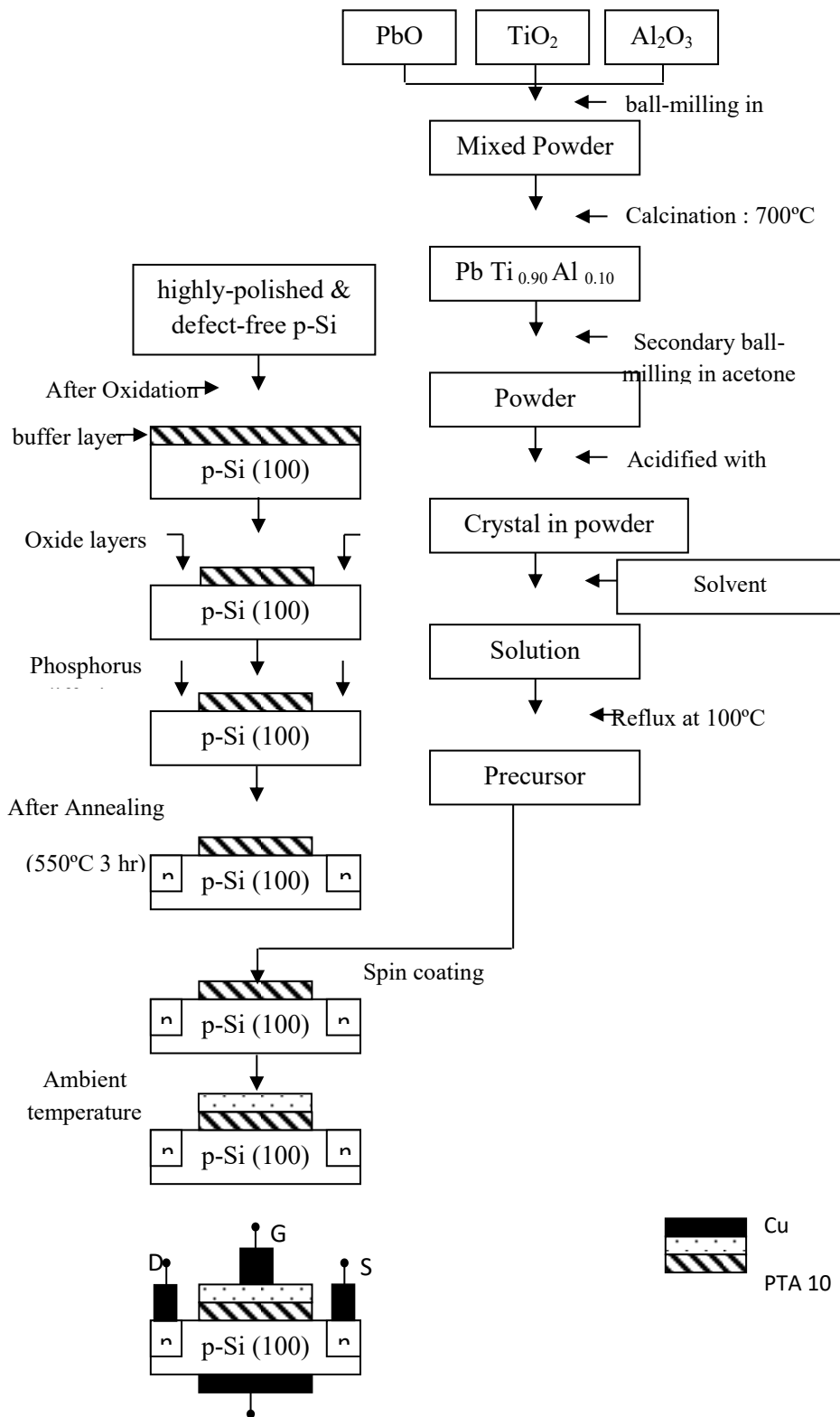[4] Lecturer, Department of Physics, Hinthada University

Figure 1. Block diagram of TFT with PTA gate material

The middle zones of the insulating layers grown on Si wafers were covered with apiezon wax and their ends were etched with HF: DIW (1:3) to remove SiO_2 layers totally. To fabricate source (S) and drain (D) regions, n-type phosphorus was deposited on these layers, annealed at 550°C for 3hr.

Thus phosphorus was allowed to enter Si by diffusion mechanism. To form the gate (G) region, the precursor solutions were spin-coated onto middle zones of the substrates while

S and D regions were masked with apiezon wax. To define the thin layers, cells were calcined at 500ºC, 550ºC, 600ºC, 650ºC, and 700ºC for 1hr. Cu electrodes were attached with S, G and D regions and back-side of the Si-wafer. In this paper, it involved the transfer characteristics of FeFET with PTA 10 gate material. The schematic representation of preparation for PTA 10 FeFET was shown in Figure 1.

RESULTS AND DISCUSSION

As the transfer characteristics, the drain to source current flow and gate to source voltage variation were measured at the saturation mode and shown in Figure (2)(a~e). The drain current was exponentially enhanced with increasing gate to source voltage at the fixed drain voltage. At the low gate voltage region, I~V variation was formed and I~V^2 variation was caused at high gate voltage region. Threshold voltages were estimated, 5.5 V, 5.3 V, 5.2 V, 5V and 4.5 V for respective cells.

From transfer characteristic curves, the graph obeyed the equation

$$I_D = k (V_{GS}-V_{TH})^2$$

Where, I_D= drain current

k = constant

V_{GS} = Gate to source voltage

V_{TH} = threshold voltage

To examine the power of ($V_{GS}-V_{TH}$), we set the unknown m and equation became.

$$I_D = k(V_{GS}-V_{TH})^m$$

By using two unknown equations, m^{th} power was formed as follows,

$$I_{D1} = k(V_{GS1}-V_{TH})^m \qquad ---------------------- \quad (1)$$

By setting , V_{GS1} =9.14 V, I_{D1} = 0.21 mA

$$I_{D2} = k(V_{GS2}-V_{TH})^m \qquad ---------------------- \quad (2)$$

By setting , V_{GS2} =8.3 V, I_{D2} = 0.11 mA

(1) ÷ (2) , we got m = 2.46

The calculated m^{th} power values were 2.46, 2.31, 2.29, 2.12 and 2.34 for respective cells. V_{TH} and m^{th} power were listed in Table (1). Temperature dependence of V_{TH} and m^{th} power were also plotted at Figure 3.

Table 1. V_{TH} and m^{th} power of TFT at different temperatures

Process Temperature	V_{TH} (V)	m^{th} power
(500ºC)	5.5	2.46
(550ºC)	5.3	2.31
(600ºC)	5.2	2.29
(650ºC)	5.0	2.12
(700ºC)	4.5	2.34

To find the transconductance values of fabricated cell, $I^{\frac{1}{m}} \sim V_{GS}$ variation was studied and shown in Figure(4)(a~e). All variations were found to be linear relationship. The transconductance value g_m was obtained from the slope of linear graph ($g_m = \dfrac{\Delta I_{DS}}{\Delta V_{GS}}$). The calculated transconductance values were listed in Table (2). The dispersion of g_m with different process temperatures was pictured at Figure 5.

Table 2. g_m of TFT at different process temperatures

Process Temperature	g_m (mA/V)	Std. Error
(500ºC)	0.0444	0.0048
(550ºC)	0.0473	0.0051
(600ºC)	0.0478	0.0051
(650ºC)	0.0002	0.0001
(700ºC)	0.0514	0.0055

To check the device quality, μ_n (mobility) was also observed at different process temperatures. The μ_n could be calculated from equation.

$$\mu_n = \frac{J_D}{qN_d\varepsilon}$$

The change in μ_n with different process temperatures was shown in Figure (6). These values were collected in Table (3).

Table 3. Mobility at different process temperatures

Sample	$\mu_n (cm^2 / Vs)$
PTA 10 (500ºC)	0.4449
PTA 10 (550ºC)	0.4939
PTA 10 (600ºC)	1.1676
PTA 10 (650ºC)	0.6948
PTA 10 (700ºC)	1.5900

The maximum current densities ($J_{D, max}$) were also observed 1.12 Acm^{-2}, 1.4 Acm^{-2}, 1.78 Acm^{-2}, 2.18 Acm^{-2} and 2.64 Acm^{-2} respectively. These values and threshold voltage (V_{TH}) were expressed with different temperature in Table (4).

Table 4. V_{TH} and $J_{D, max}$ at different process temperature.

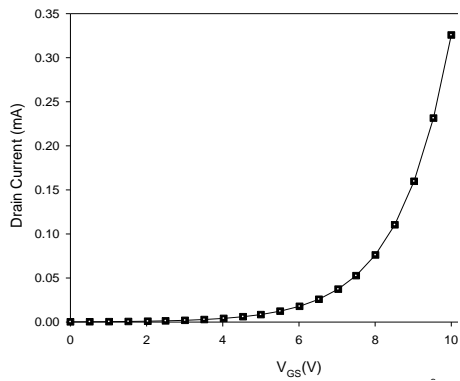| Sample	$V_{TH}(V)$	$J_{D,max}$ (Acm^{-2})
PTA 10 (500ºC)	5.5	1.12
PTA 10 (550ºC)	5.3	1.40
PTA 10 (600ºC)	5.2	1.78
PTA 10 (650ºC)	5.0	2.18
PTA 10 (700ºC)	4.5	2.64

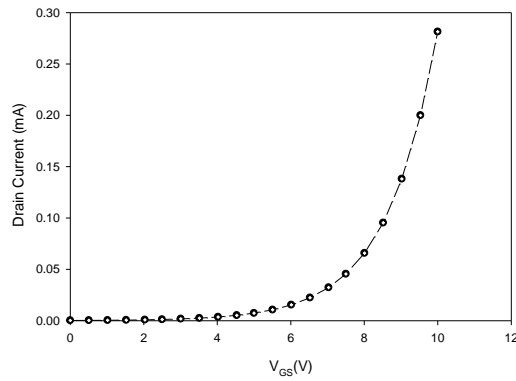Figure 2(a). Transfer Characteristics of TFT at 500°C

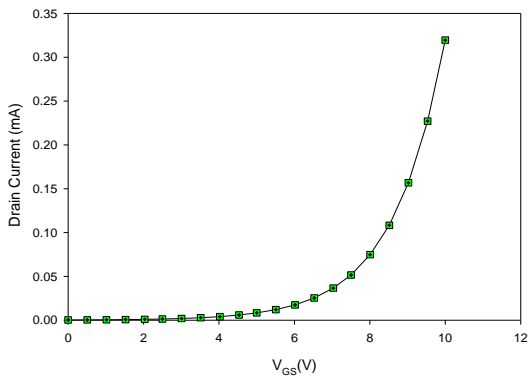Figure 2(b). Transfer Characteristics of TFT at 550°C
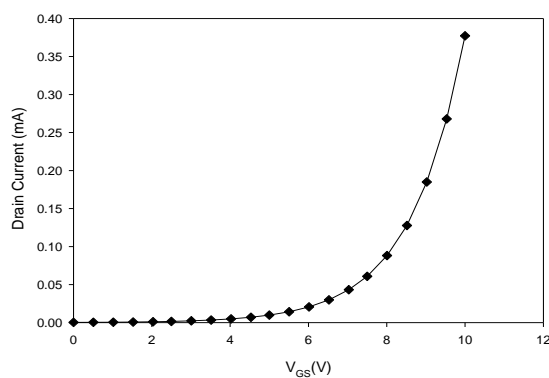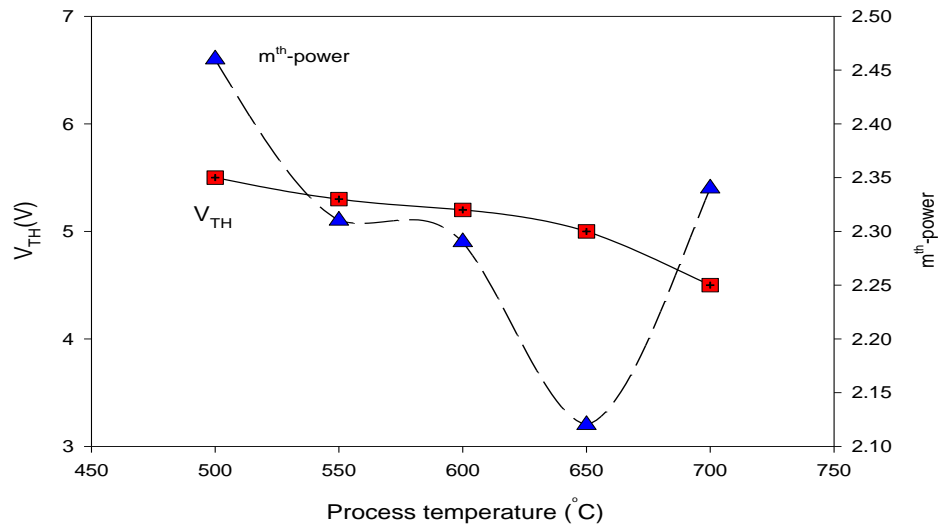

Figure 2(c). Transfer Characteristics of TFT at 600°C

Figure 2(d). Transfer Characteristics of TFT at 650°C
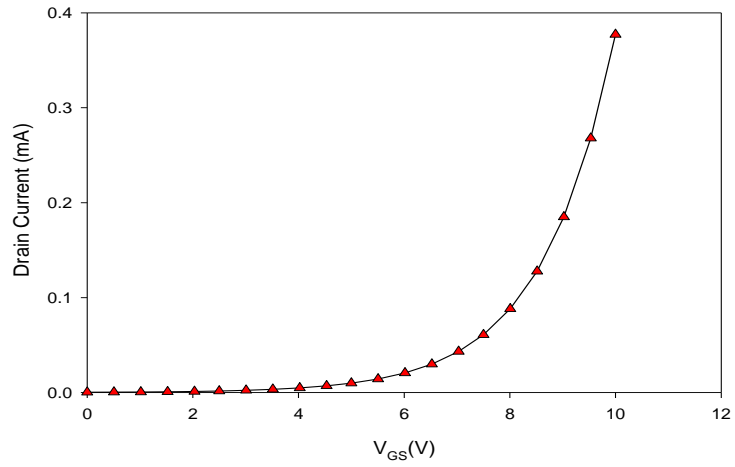
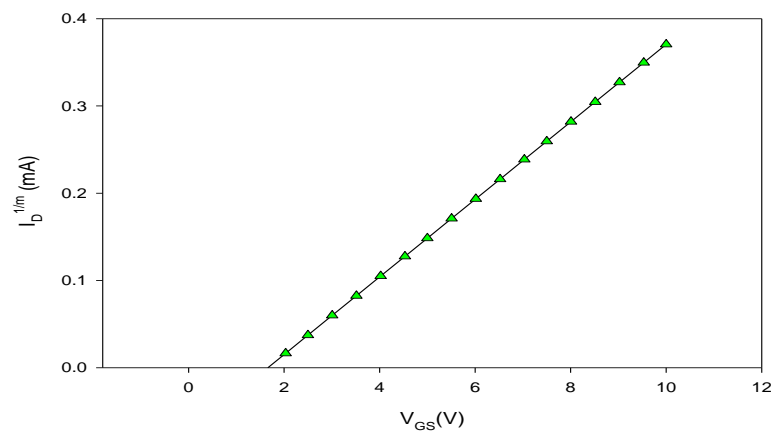Figure (3) Temperature dependence of V_{TH} and m^{th} power for PTA 10 gated TFT

Figure 4(a) Transconductance Characteristic of TFT at 500°C
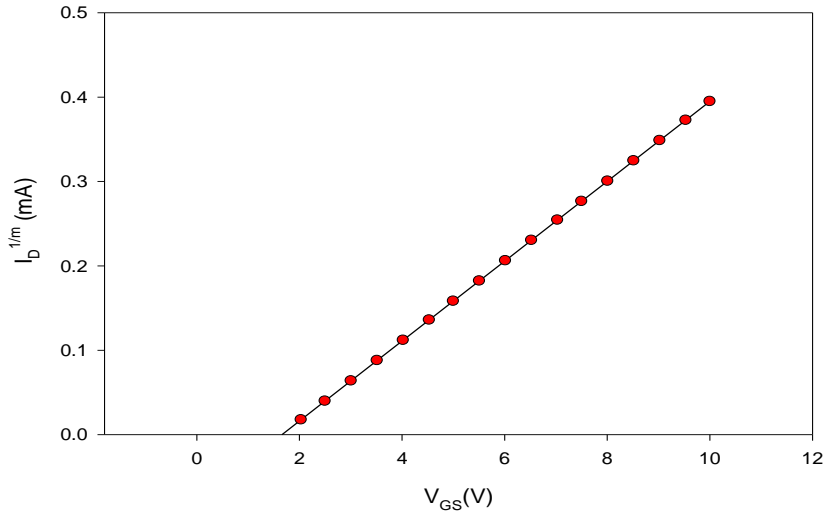
Figure 4(b) Transconductance Characteristic of TFT at 550°C
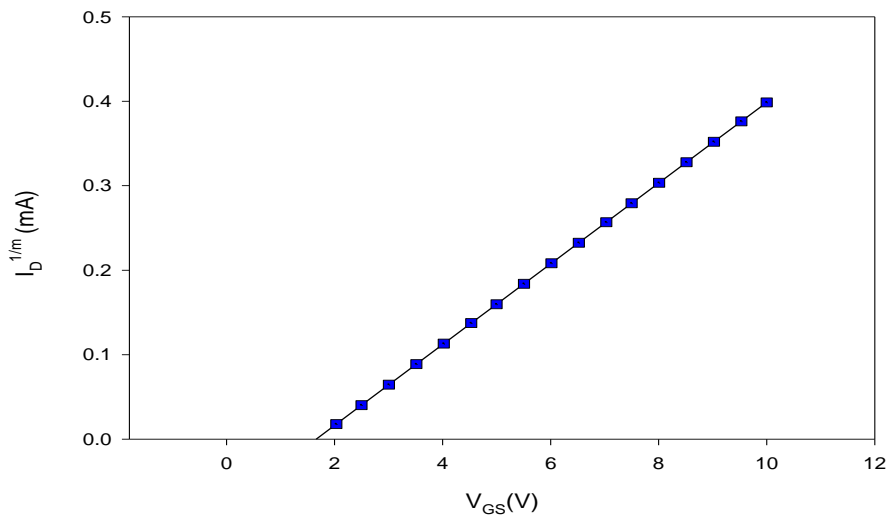

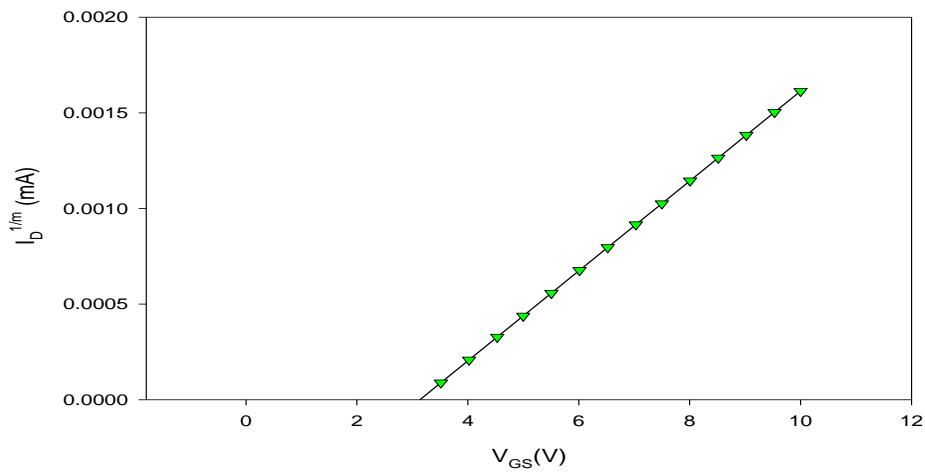Figure 4(c) Transconductance Characteristic of TFT at 600°C

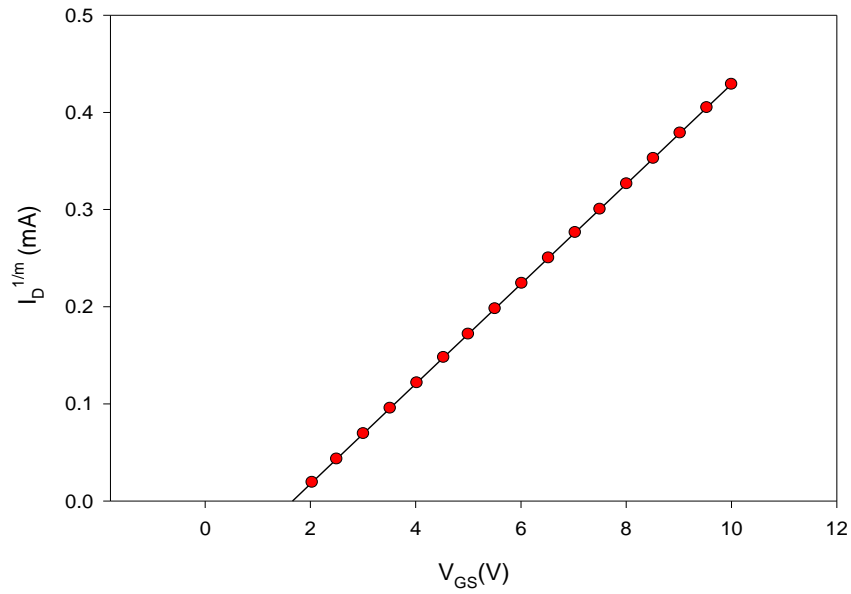Figure 4(d) Transconductance Characteristic of TFT at 650°C

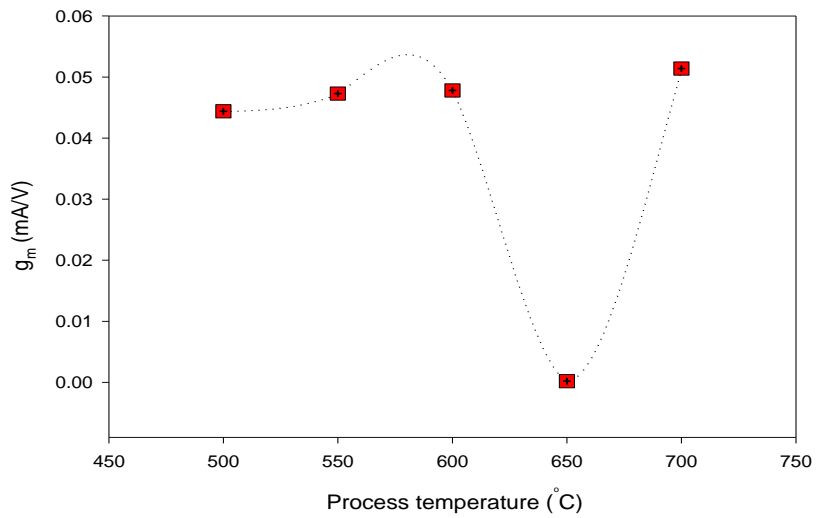Figure 4(e) Transconductance Characteristic of TFT at 700°C

Figure (5) Temperature dependence of transconductance value for PTA 10 gated TFT
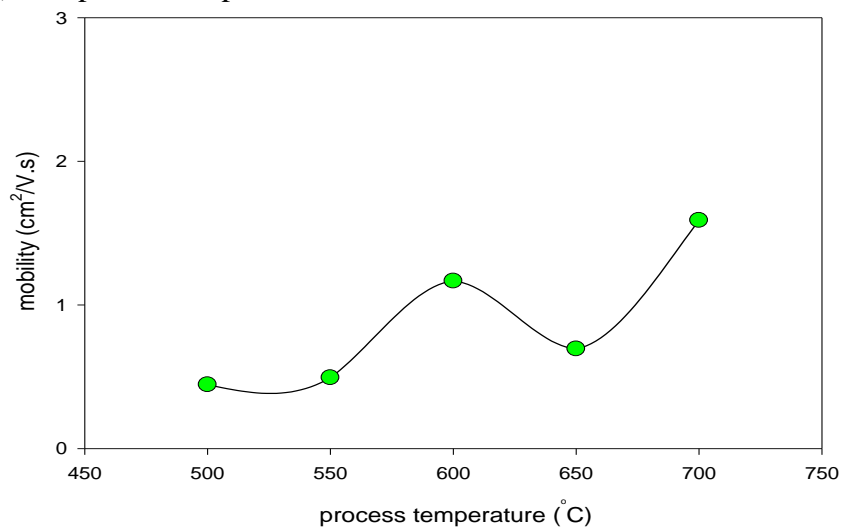

Figure (6) Change in mobility with different temperatures

CONCLUSION

In this research the transfer characteristics of the Al modified $PbTiO_3$ TFT were studied first. Then, Processing parameters were systematically observed in this study. Eventually, the results obtained were salient conclusions that they were following:

(i)   The PTA epilayer were successfully deposited on n+ introduced Si substrate using spin-casting method.

(ii)   As the transfer characteristics, $I_D \sim V_{GS}$ and $I_D \sim V_{GS}^2$ variation were caused at low and high gate voltage regions on transfer curve for all fabricated cells.

(iii)   According to the mth power measurement, it was obvious that I_D was directly proportional to $(V_{GS}-V_{TH})^{m=2}$ and revealed the parabolic nature of transfer curve.

(iv) g_m was obtained from $I_D^{\frac{1}{m}} \sim V_{GS}$ linear relationships and these values were accepted for FeFET field and

(v)   Mobility of all fabricated TFT were observed and found to be within the range of accepted values for 1T of FRAM. Accordingly, the TFT has the highest μ_n at 700℃.

References

A.HOSSEEINI, K.C.ICLI, M.OZENBAS, C.ERCELEBI, "Fabrication and charactrrization of spin-coated TiO_2 films"*Energy Procedia ,* Vol.60,pp.191-198,2014.

P.Sudheendra, A.O.Surendranathan, N.K. Udayashankar," Titanium-Aluminium Thin Films Preparation By Oblique Angle Sputtering And Their Characterization", International Journal of Engineering Research & Technology", Vol.1,pp.1-5, Oct.2012.

W.L.Jung, J.Y.Sun, H.L. Seong, " *Optical and Electrical Properties of $Al_xTi_{1-x}O$ Films*, Vol.56, No.1, pp.96-99,Jan. 2010.

Z.Essalhi, B.Hartiti, A.Lfakir, M.Saidat, P.Thevenin, " *Optical prpperties of TiO2 Thin films prepared by Sol Gel method*", J.Mater.Environ.Sci." Vol.7, No.4, pp.1328-1333, 2016.